layer 3 is performed between the highly doped silicon layers 8a and 8b and the CoSiz layers 9a and 9b only."

In the Claims:

Applicants elect the Group I invention including claims 1-16 for further examination on the merits. This election is without traverse.

Please cancel claims 17-22 without prejudice or disclaimer of the subject matter contained therein.

The following replacement claims are respectfully submitted:

1. (Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers formed in regions which are respectively in contact with the channel region in the source region and the drain region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively in contact with the pair of impurity layers, wherein bottom surfaces of the pair of metallic silicide layers extend to bottom surfaces of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:

$$(X / Y) > (X0 / Y0).$$

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5. (Amended) A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region defined by the source region and the drain region;

a pair of impurity layers formed into regions which are respectively in contact with the channel region in the source region and the drain region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively in contact with the pair of impurity layers, wherein the pair of metallic silicide layers have a thickness which is equal to or more than 80% thickness of from the upper surface of the metallic silicide layers to the bottom surface of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:

$(X / Y) > (X0 / Y0)$.

9. (Amended) A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first impurity layer and the first metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide layer, wherein the second impurity layer and the second metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity layer and the second impurity layer,

wherein the first metallic silicide layer and the second metallic silicide layer are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:

$$(X / Y) > (X0 / Y0).$$

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13. (Amended) A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first metallic silicide layer has a thickness which is equal to or more than 80% a thickness of from an upper surface of the first metallic silicide layer to a bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide layer, wherein the second metallic silicide layer has a thickness which is equal to or more than 80% a thickness of from an upper surface of the second metallic silicide layer to a bottom surface of the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity layer and the second impurity layer,

wherein the first metallic silicide layer and the second metallic silicide layer are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality:

$$(X / Y) > (X0 / Y0).$$